Center for Innovative Photonic Chip-scale Technologies:

Systems-on-a-Chip Research

Mike Haney, ***George Mason University***

Fairfax, VA, USA 22030-4444

mhaney@gmu.edu

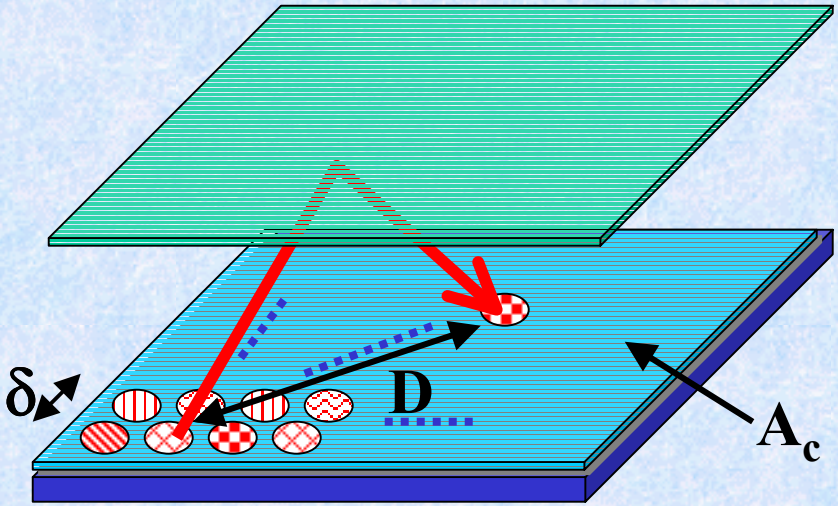
University Opto Centers Kickoff Meeting

November 9, 2000, Dana Point, CA

Motivation

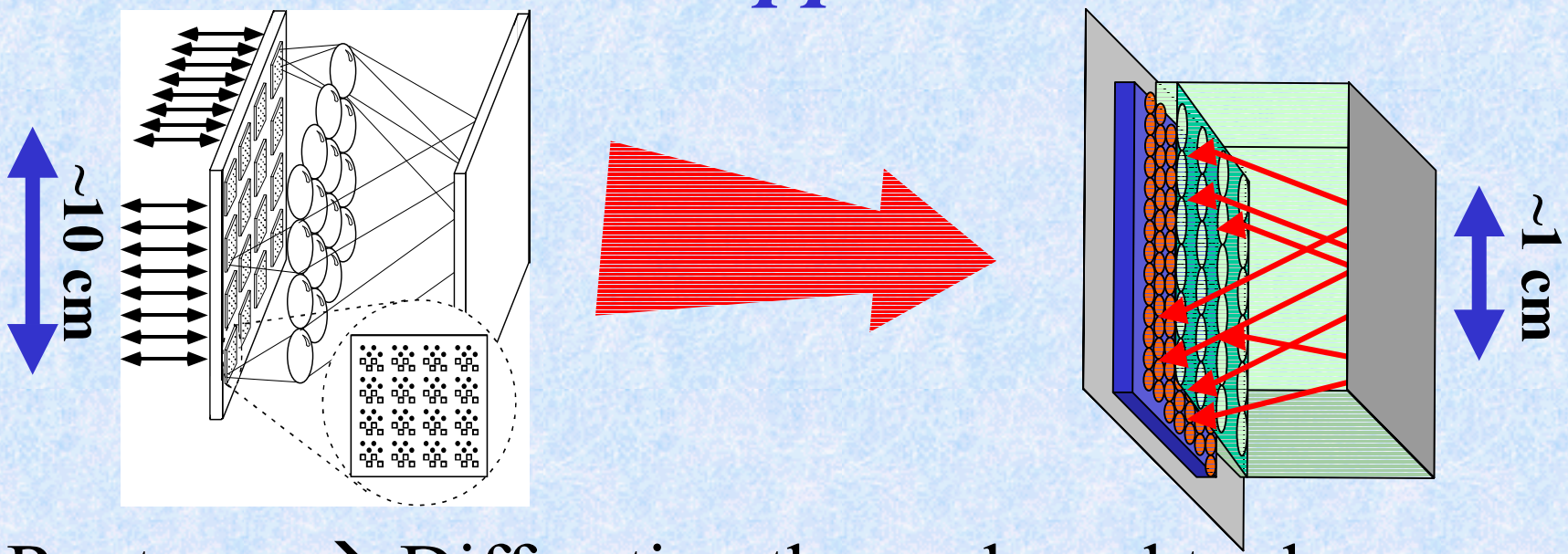
- Si technology is moving toward billions of devices/chip with multi-Gbit/s rates → **SOC**.
- Fundamental interconnect problems will scale down to intra-chip level → **can optics help?**
- Opportunity to influence SOC development at early phase.
- OE technology rapidly advancing → **it's *not too soon* to think about applications.**

Limits of Point-to-Point Global FSOI Single Hop Fabrics



- $D_{max} \cong \delta^2/4\lambda$
- $A_c \cong D_{max}^2$
- $Density_{I/O} = 1/\delta^2 \cong 1/4(\lambda(A_c)^{1/2})$
- $I/O_{max} \cong (A_c)^{1/2}/4\lambda$ e.g., $I/O_{max} \cong 8000$ for A_c=10 cm^2

Scaling Photonics Technologies for SOC Applications



Raytrace → Diffraction theory based tools

μ-optics → meso-optics → …..

VCSELs → Quantum dots

Waveguides → PBG structures

2-D PBG → 3-D PBG

Approach

- Determine problem domains that can leverage high-density SOC architectures.
- Scale architectural solutions to the chip level and quantify the benefits.
- Determine key areas for study -- provide input to technology efforts.
- Leverage technology developments and projections into architectural concepts.
- Perform end-to-end performance analyses.

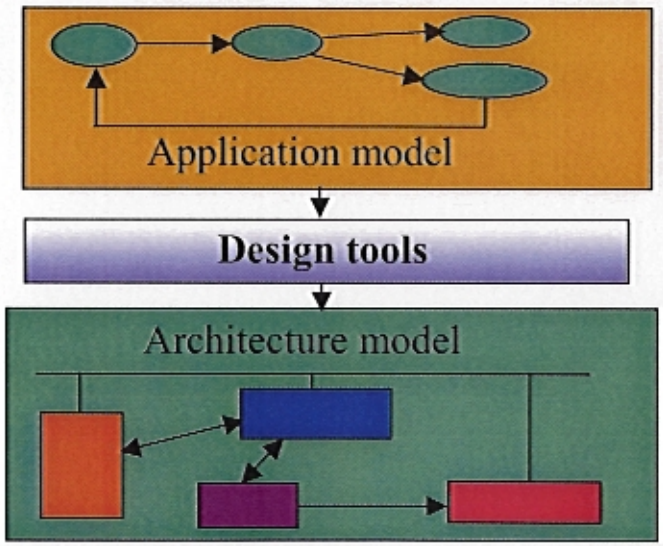
Projects

1. **Application Mapping based on Optical Interconnections for SOC**

2. **Electronic/Photonic Integration**

Application Mapping for Embedded Multiprocessors

- computing systems that perform well defined functions
- usually "reactive" in nature (e.g. radar, mobile communications)



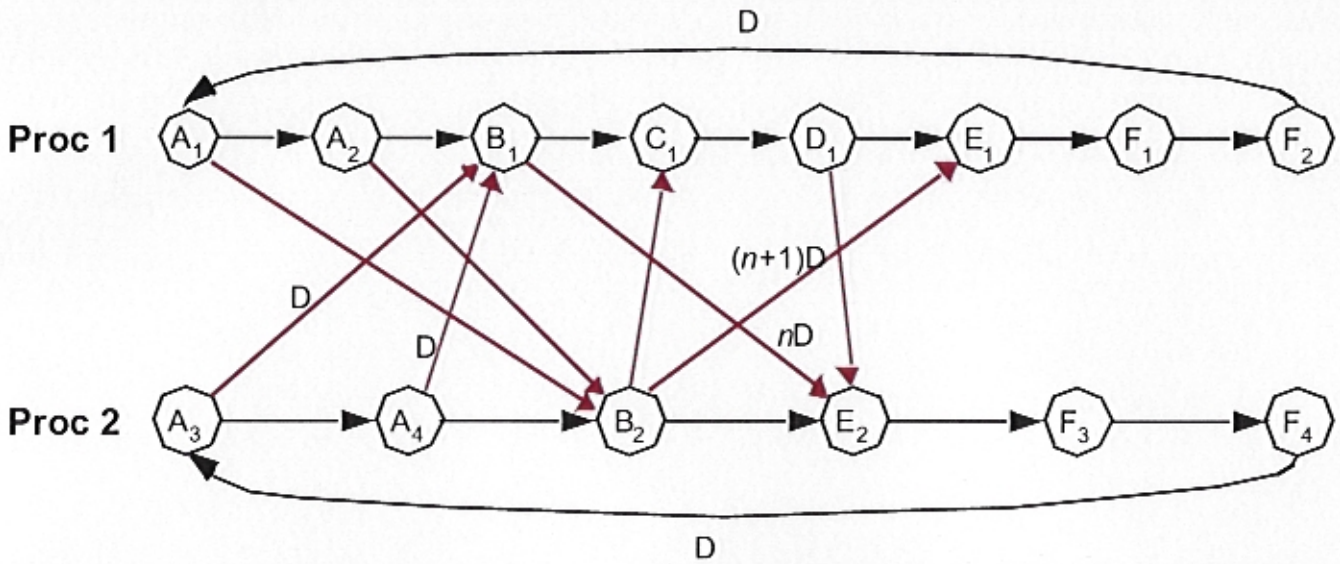
- Selection of architecture template
- Allocation of template resources
- Assignment of tasks to processors
- Ordering of tasks on processors
- Optimization of interprocessor communication and synchronization

Requires efficient techniques for performance estimation and design space exploration

Performance Estimation for Multiprocessor DSP

Key Complication:

Continuous operation on vast data streams

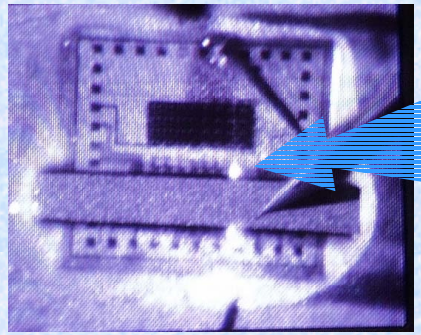


"Synchronization Graph" Model

(four-channel multi-resolution QMF filter bank)

Becomes increasingly accurate as communication cost and contention are reduced

Baseline Photonic Integration Technologies



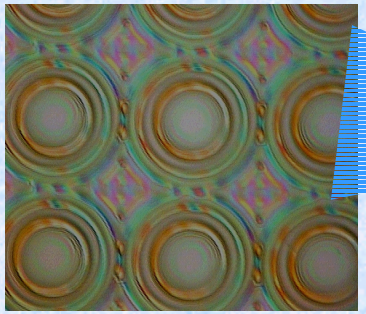
VCSELs integrated with SOI

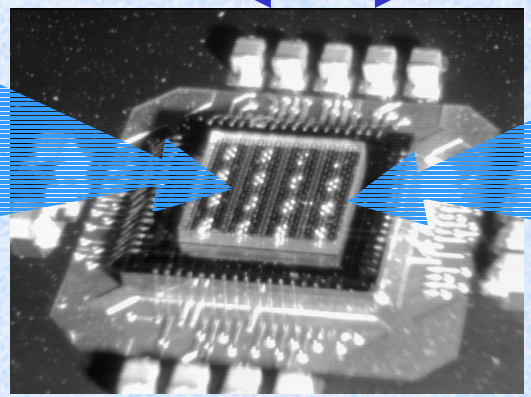
5 mm

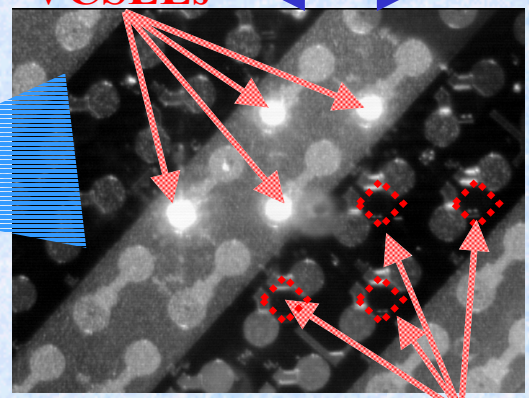
200 µm

VCSELs

DOE array

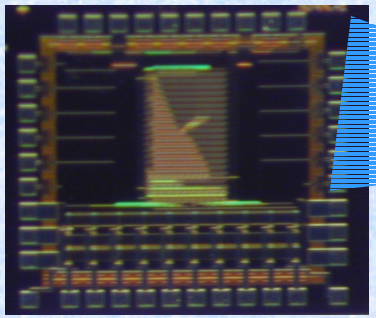


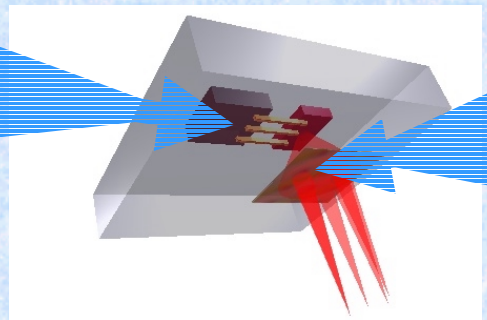


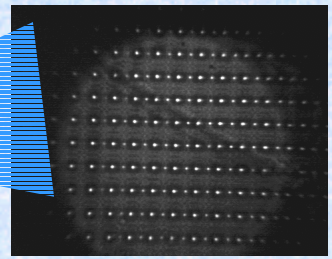


Detectors

VCSEL Driver

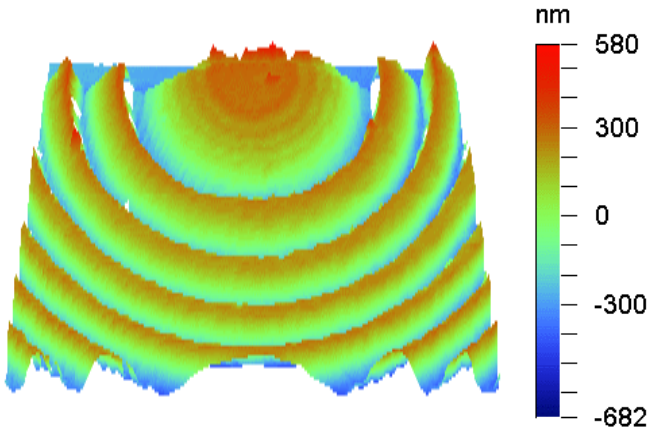




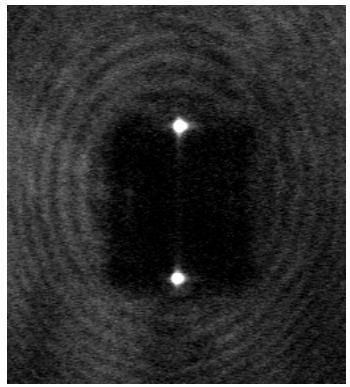


Beam Fan-Out

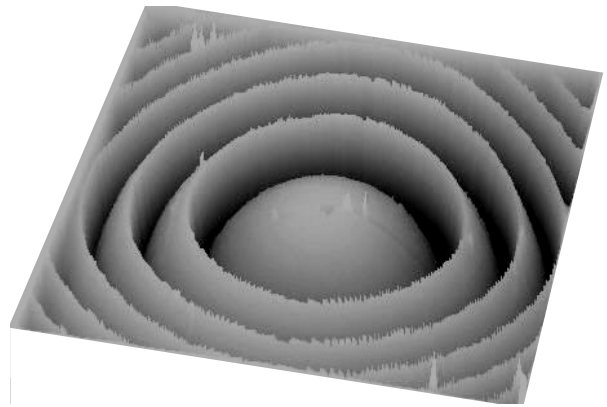
Electromagnetic Design and Fabrication of 3-D Mesoscopic Diffractive Optical Elements



(a)



(b)

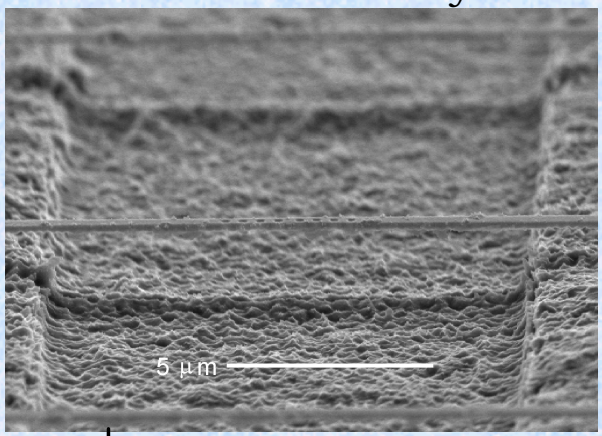


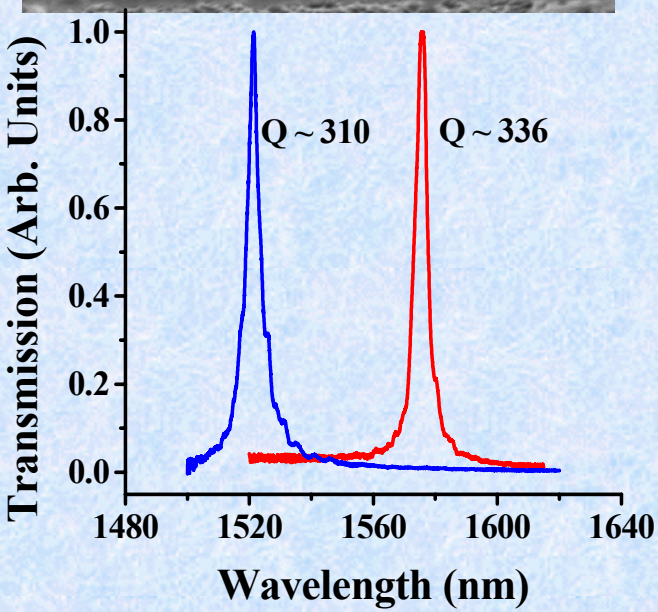
(c)

(a) Surface profile of a multilevel 1-to-2 fanout mesoscopic DOE
(b) Experimental reconstruction of the meso-DOE at the design focal length of 500μm
(c) Fresnel lens of 128 μm square for a focal length of 1mm (3D-AFM image)

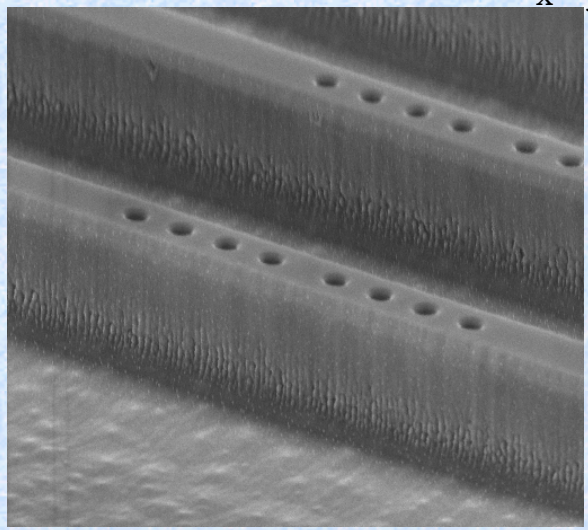
1D and 2D Photonic Bandgap Guides/Microcavities

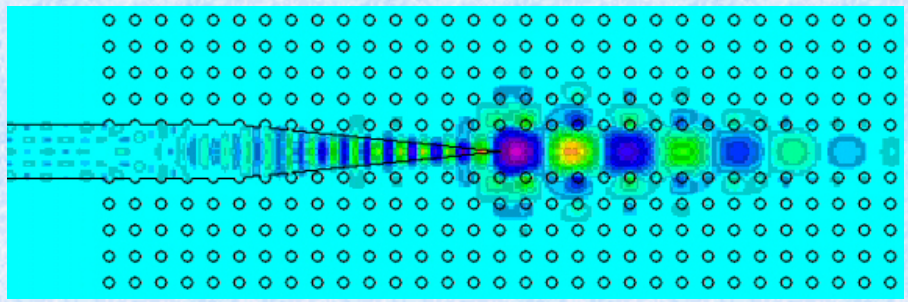
Airbridge PRG microcavity:
GaAs surrounded by air





Monorail PBG GaAs-on-Al_xO_y





Coupling from normal dielectric waveguide into a photonic crystal waveguide

Photonic Interconnects for SOC

"Application Specific" Network

- Customized interconnection fabric.

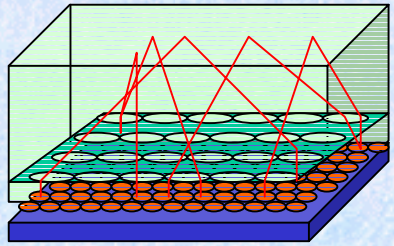
"Place and Route"

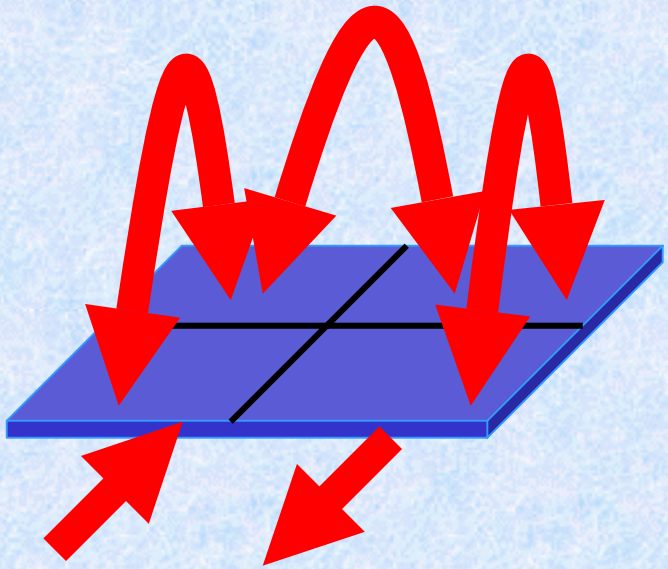
"Chip Area Network"

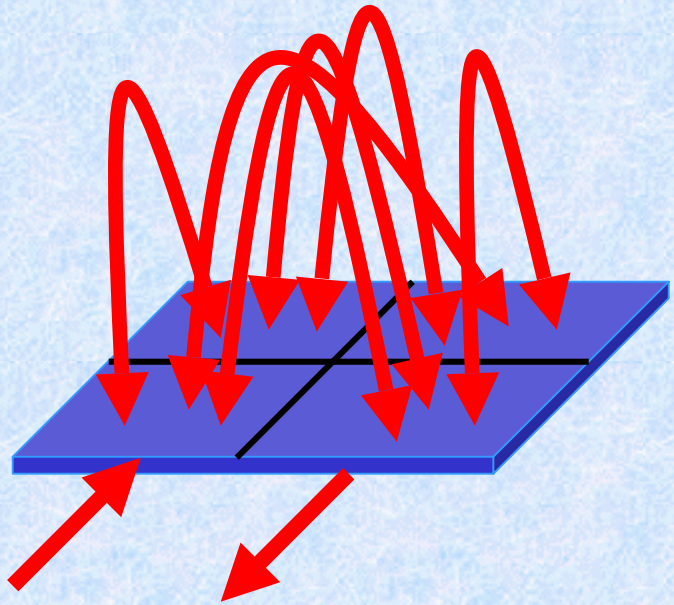
- Generic fabric for wide class of interconnect-bound applications.

"Route and Place"

Photonic SOC Architectures







"Fire-hose" Architectures

High Aggregate BW

"Fountain" Architectures

High Min. Bisection BW

Photonic SOC Research Issues

- Application mapping and performance estimation tools.
- Interconnection architecture analysis and implementation.
- Diffractive optical element design and fabrication.
- Active/passive alignment, integration, packaging.
- 2-D/3-D interface.
- Transceiver power management and related thermal issues.
- Throughput/Crosstalk analysis and measurement.

Summary

Overall Goal:

- Provide linkage between integrated photonic technologies and applications….

….in order to push OE interconnect architectures and algorithms into the chip-scale domain.